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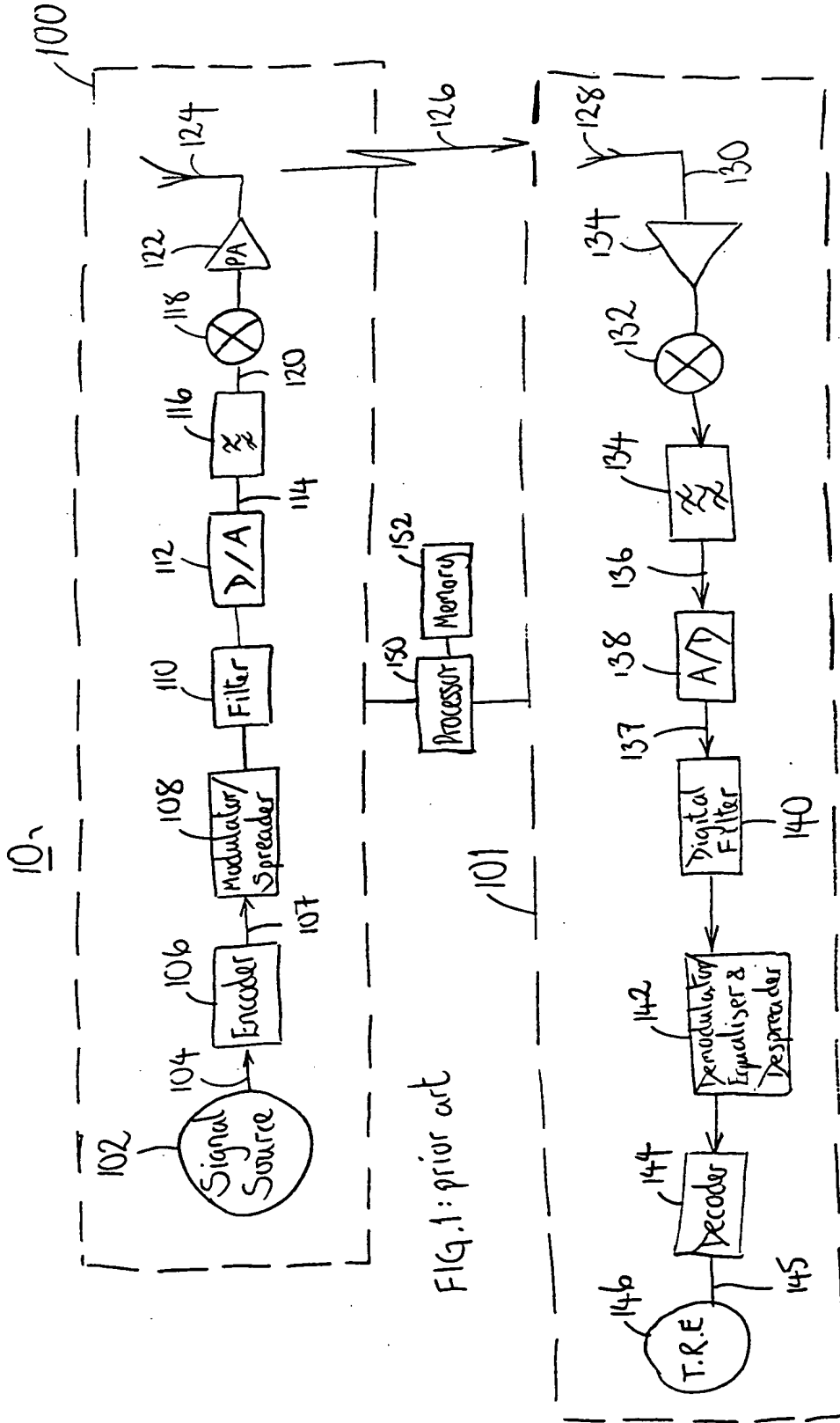
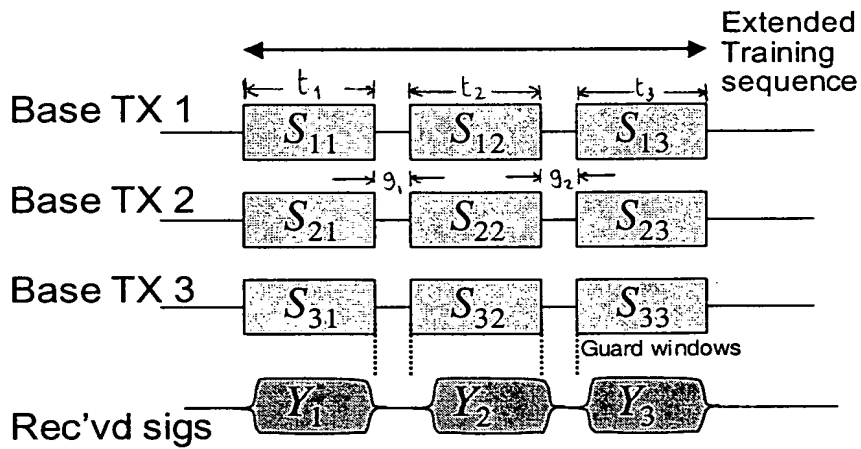
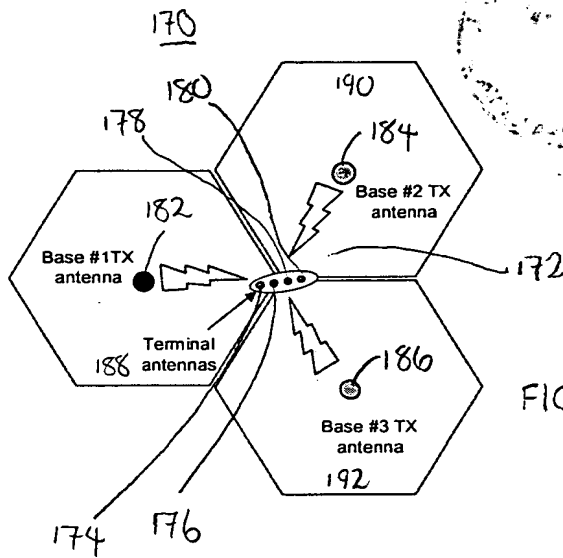


FIG. 1: prior art



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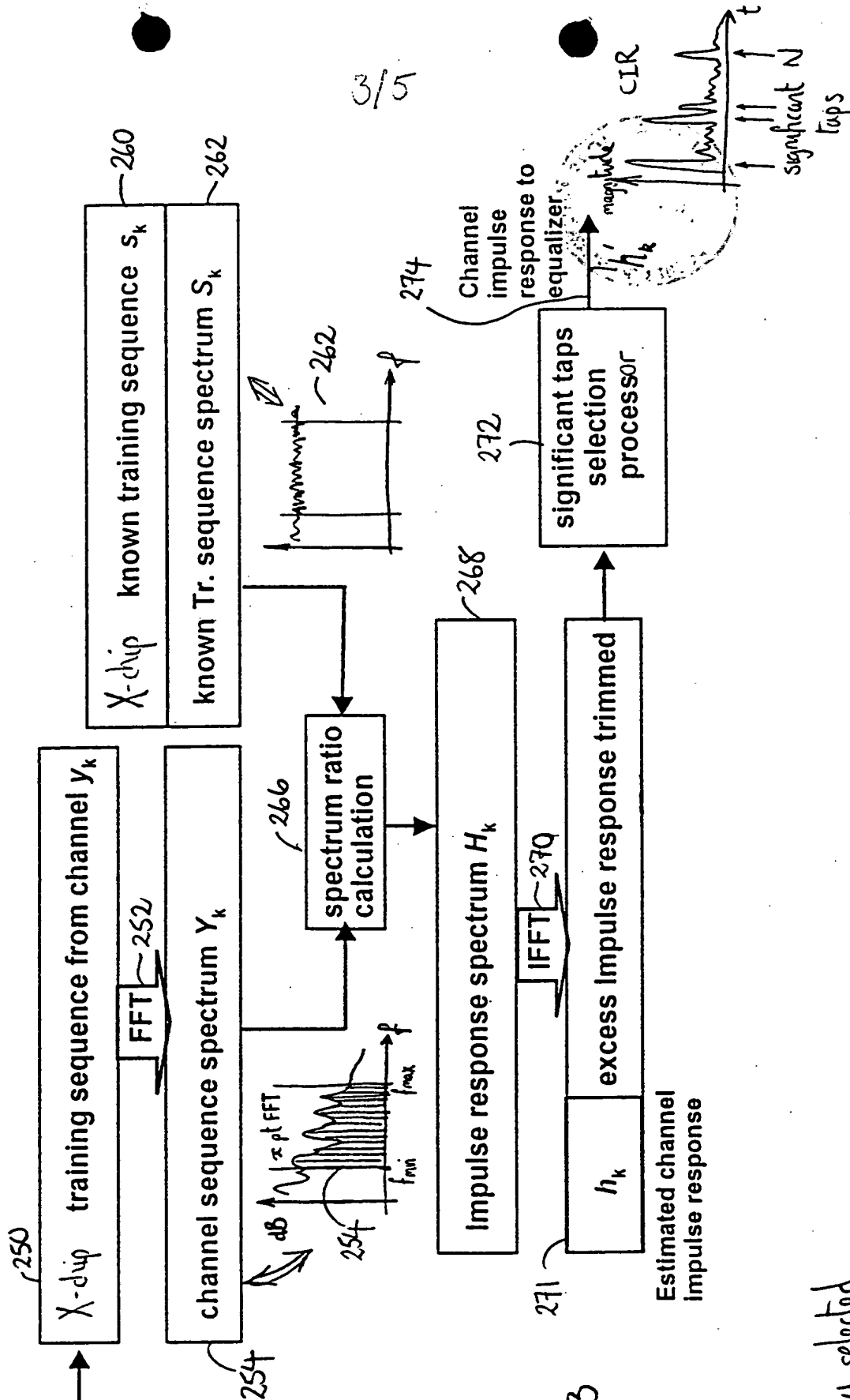
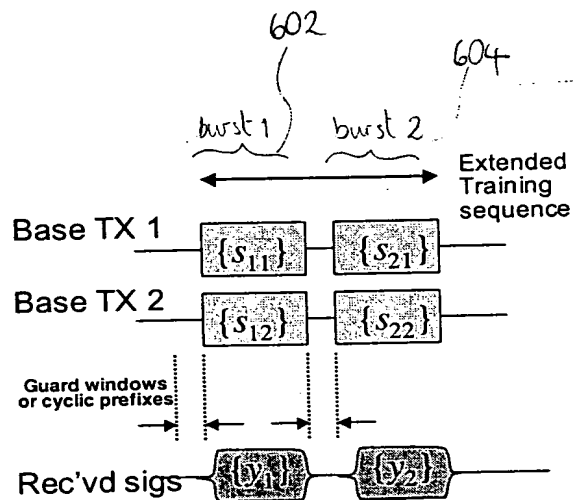
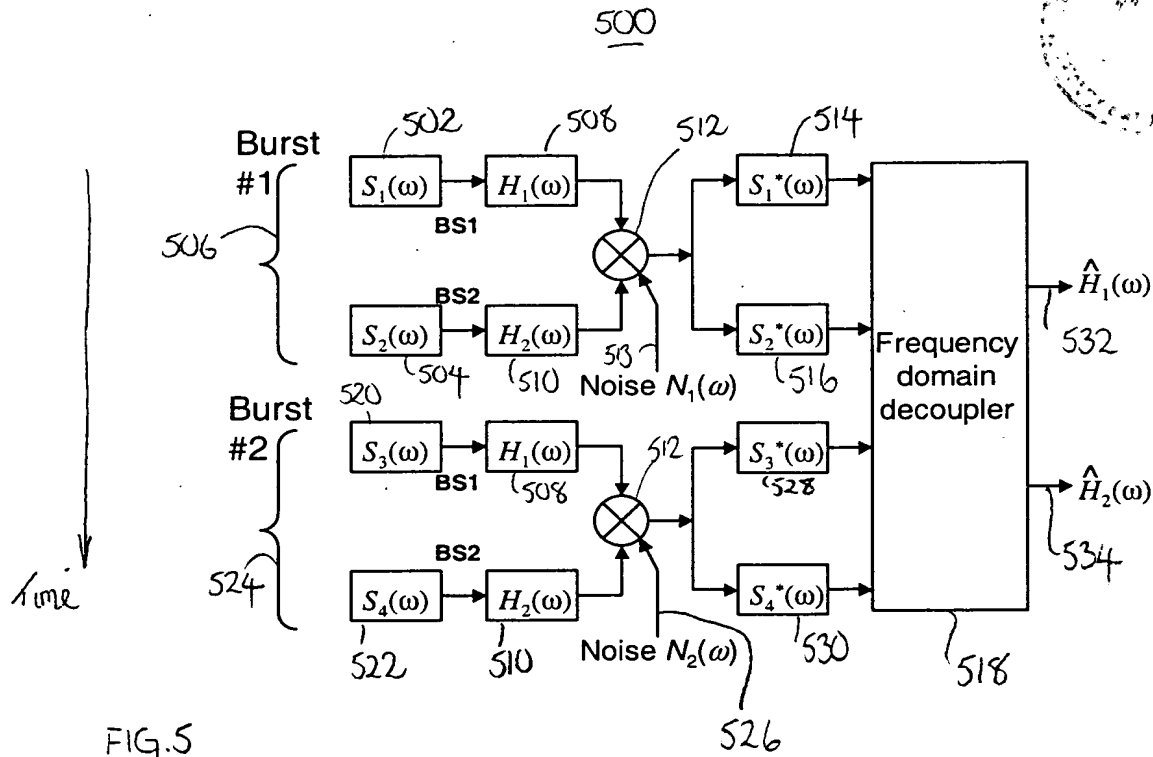


FIG. 3

X=arbitrary selected number of chips in training sequence set by system standard.



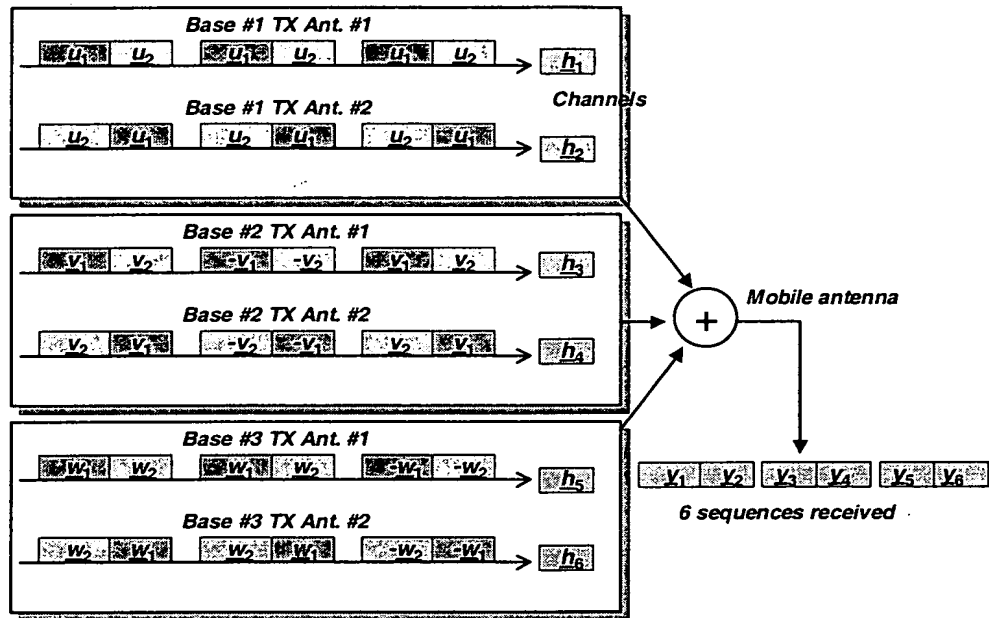


FIG.7